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3-November 2007

VESA DisplayPort™
Phy Compliance Test Standard Version 1
Agilent Method of Implementation (MOI) for DisplayPort Sink Compliance Tests
Using Agilent J-BERT N4903A or Agilent 81250 ParBERT

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MODIFICATION RECORD

November 03, 2007 (Version 1.0)
Michael Herz: minor updates after CTS version 1 release

October 19, 2007 (Version 0.84)
Sebastian Mezger: improved ParBERT part list

October 16, 2007 (Version 0.83) added Appendix C
Sebastian Mezger: added Appendix C, describing the ParBERT Resource Requirements

October 4, 2007 (Version 0.82) added Appendix D
Sebastian Mezger: added Appendix D, describing how to use Agilent's Test Automation Software N5990A, together with the ParBERT

September 28, 2007 (Version 0.81) INITIAL DRAFT RELEASE
Michael Herz: Initial Release

SINK COMPLIANCE TESTS

Overview:

This group of tests verifies receiver functionality under stressed-signal conditions, for the purposes of performing DisplayPort Interoperability Testing. This test is limited to functionalities which are covered by the VESA compliance test specification (Section 4 of the VESA DisplayPort PHY Compliance Test Standard, Version 1), and do not provide comprehensive coverage of all receiver tolerance requirements defined by the DisplayPort Standard v1.1 specification.

Sink Jitter Tolerance Test (Normative)

Purpose: To verify that the receiver of the sink device under test (DUT) can operate within the required bit error ratio under stressed signal conditions.

References:

[1] VESA DisplayPort PHY Compliance Test Standard, Version 1, Section 4
[2] VESA DisplayPort Standard, Version 1.1

Resource Requirements: Using J-BERT N4903A see Appendix A and using 81250 ParBERT see Appendix C.

Last Modification: November 3, 2007

Discussion:

- Reference [1] specifies the basic requirements for Receiver Jitter Tolerance testing, for the purpose of the DisplayPort interoperability program. These requirements are a subset of the complete set of requirements defined in the DisplayPort specification.
- The test procedure requires to operate the device under test and refers to the AUX channel and internal DPCD registers. See reference [2] for details. Due to the lack of an appropriate test tool a vendor specific tool is needed to perform these steps.
- Step (1) of the test procedure uses sinusoidal jitter (Sj) at the highest required test frequency as stated in reference [1]. Later on the Sj shall be changed to the actual test frequency.
  In order to simplify the test procedure the calibrated amount of Sj at the actual test frequency may be used instead. If the device under test cannot achieve frequency lock or symbol lock under the modified procedure the test is not failed but has to be repeated using Sj at the highest frequency.

Test Setup: Using J-BERT N4903A see Appendix A and using 81250 ParBERT see Appendix C.

Setup Calibration: Using J-BERT N4903A see Appendix B and using 81250 ParBERT see Appendix D.

Test Procedure:

Note this test procedure assumes the user has already performed the initial system setup and calibration procedures outlined in Appendices A-B respectively Appendices C-D of this document.

1) Connect the SSG to the lane under test and clock pattern generator to the adjacent lanes. Adjust data rates for Reduced Bit Rate or High Bit Rate. All jitter sources and minimum eye were calibrated previously. Inter-symbol interference (ISI) and random jitter (Rj) are turned on. Sj is turned on at the highest frequency (i.e 100MHz for HBR and 20 MHz for RBR).

Frequency lock phase

2) SSG outputs a D10.2 clock pattern (includes injected ISI, Rj and Sj jitter).
3) AUX Control initiates the frequency lock phase
4) 4. After >100µs AUX Control verifies whether DUT achieved frequency lock. If not go to the previous step. If frequency lock cannot be achieved within 5 retries (with maximum consecutive AUX Defers allowable = 8) the test result shall be a failure. Lock is verified by polling CR_LOCK status for the data lane under test:
   If LANE0_CR_DONE (Address202h bit 0) = 1
   If LANE1_CR_DONE (Address202h bit 4) = 1
   If LANE2_CR_DONE (Address203h bit 0) = 1
   If LANE3_CR_DONE (Address203h bit 4) = 1

Symbol lock phase

5) SSG outputs symbol lock pattern as defined in specification with ISI, Rj and Sj jitter injected
6) AUX Control initiates the symbol lock phase

7) After >100µs AUX Control verifies whether DUT achieved symbol lock. If not go to the previous step. If symbol lock cannot be achieved within 5 retries (with maximum consecutive AUX Defers allowable = 8) the test result will be a failure. Lock is verified by polling CR_LOCK status for the data lane under test:
   If LANE0_CHANNEL_EQ_DONE (Address202h bit 1)
   If LANE0_SYMBOL_LOCKED (Address202h bit 2)
   If LANE1_CHANNEL_EQ_DONE (Address202h bit 5)
   If LANE1_SYMBOL_LOCKED (Address202h bit 6)
   If LANE2_CHANNEL_EQ_DONE (Address203h bit 1)
   If LANE2_SYMBOL_LOCKED (Address203h bit 2)
   If LANE3_CHANNEL_EQ_DONE (Address203h bit 5)
   If LANE3_SYMBOL_LOCKED (Address203h bit 6)

PRBS7 counter test phase

8) SSG outputs PRBS7 pattern as defined in specification with ISI, Rj and Sj jitter injected
9) AUX Control initiates and clears the PRBS7 error counter
10) SSG injects one single bit error while looping the PRBS7 pattern (I.e. in subsequent repetitions of the PRBS7 pattern only once the PRBS7 pattern shows one wrong bit)
11) AUX Control verifies that the PRBS7 counter shows one bit error. If not the test result will be a failure.

BER test phase

12) Stressed Signal Generator outputs PRBS7 pattern as defined in specification with Rj, Sj, and ISI jitter injected. The Sj frequency has to be set to the current test case.
13) AUX Control clears the PRBS7 error counter
14) Run test for specified time
15) The PRBS7 error counter is read through AUX Channel Control.

Observable Results:

For each lane and all supported data rates:

- The receiver is required to achieve frequency lock and symbol lock within 5 retries.
- The PRBS7 counter has to be operational.
- For all jitter frequencies, the number of errors shall not exceed the number of allowable errors as stated in Table 4-1 in the CTS document [1]:

Data Rate	Sj Jitter Frequency	Test Time	Max. Num of Bit Errors Allowable
RBR, HBR	2 MHz	RBR = 620 s, HBR = 370 s	1000
RBR + 350ppm, HBR + 350ppm	10 MHz	RBR = 62 s, HBR = 37 s	100
RBR, HBR	20 MHz	RBR = 62 s, HBR = 37 s	100
HBR	100 MHz	HBR = 37 s	100

APPENDICES

Overview:

Test suite appendices are intended to provide additional low-level technical detail pertinent to specific tests contained in this test suite. These appendices often cover topics that are outside of the scope of the standard, and are specific to the methodologies used for performing the measurements in this test suite. Appendix topics may also include discussion regarding a specific interpretation of the standard (for the purposes of this test suite), for cases where a particular specification may appear unclear or otherwise open to multiple interpretations.

Test suite appendices are considered informative supplements, and pertain solely to the test definitions and procedures contained in this test suite.

Appendix A – General Resource Requirements using the Agilent J-BERT N4903

Purpose: To define the hardware/software requirements for performing the tests defined in this document.

References: None.

Last Modification: November 3, 2007

Discussion:

- Reference [1] does not specify whether the aggressor signals should be turned on during setup calibration. However test results have shown that cross talk effects add significant total jitter (Tj) to the stressed signal. Therefore the calibration setup will include the aggressor signals.

A.1 - Introduction

In order to perform receiver jitter tolerance testing on DisplayPort sink devices, several pieces of equipment are needed. The primary functional components are as follows:

Component	Function	Device/Model
Stressed Signal Generator (SSG)	Generates jittered/stressed test signal	Agilent J-BERT N4903. The following jitter options are required: • Rj, Pj, Sj: J10, • Interference channel: J20
Required SSG accessories	Note: some accessories may be shipped with SSG	• Short cable kit for connecting ISI ports: Agilent N4915A-002 • Adapter 3.5mm to 2.4mm: Agilent N4911A-002 (2 needed)
Jitter Measurement Device (JMD)	Used to verify/calibrate SSG output	Agilent Infiniium DSO81304A 13GHz Real-Time DSO
3-Way, 50/50 resistive Power Divider (PD)	Used to split SSG aggressor output	Agilent 11636B (2 required)
SMA test cables	Used to connect the SSG to PDs and the JMD for calibration	Agilent 15442-61601, or equivalent (set of 4 cables)
SMA to SMP test cables	Used to connect SSG with test fixture. Note: some SMA to SMP cables may be shipped with the DisplayPort test fixture.	Agilent E4809-61603 (6 required)
DisplayPort Test Fixture (TF)	Used to connect SSG with device under test	Agilent W2641A
DisplayPort Receptacle Test Fixture (RTF)	Used to calibrate test setup at compliance point	Molex part number tbd
Blocking Capacitor (BC)	Used to AC couple the SSC and DUT	Agilent 11742A (2 required)
50 Ohm termination resistors	Used during setup calibration	Agilent N4912A (4 required)

A.2- Basic Test Setup

Figure A-1 shows the test setup with the Agilent J-BERT. Connect the pattern generator output to the ISI plug-in. Mount the blocking capacitors (BC) at the ISI plug-in output. Use two of the SMA to SMP cables and connect it to the lane under test. Note that the TF is labeled for source test only. All lane numbers and signal polarity must be flipped. Use two of the SMA test cables and connect the trigger output to the power dividers (PD). The four remaining SMA to SMP cables connect to the lanes on the test fixture that are adjacent to the lane under test.

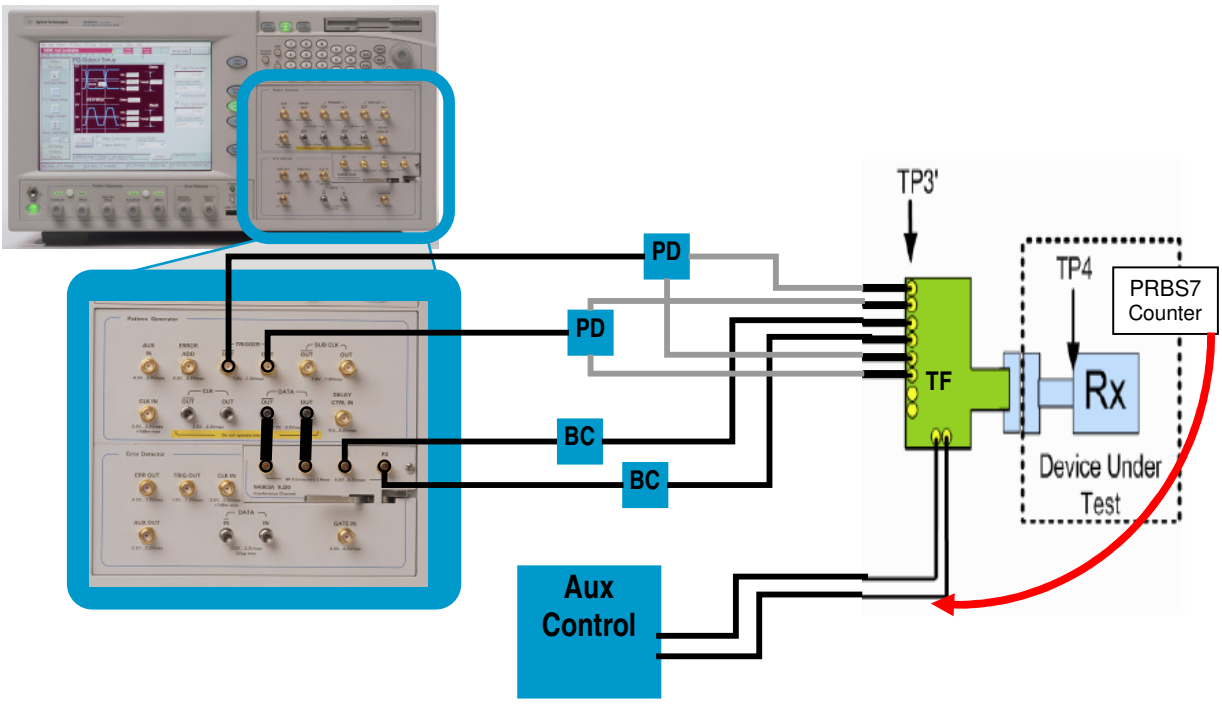

Figure A-1: Basic Test Configuration

Set J-BERT trigger output to half clock rate as shown in figure A-2.

Figure A-3 shows the test configuration with an example DUT. Since there exists no standard Aux Control tool a vendor specific tool has to be used to operate the DUT. This tool may also utilize proprietary debug interfaces.

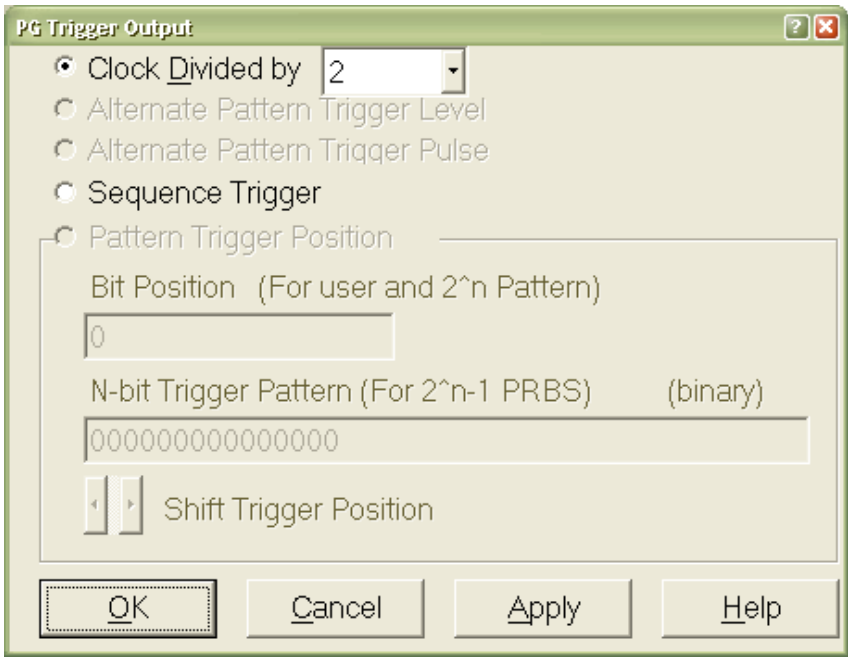

Figure A-2: J-BERT trigger configuration menu

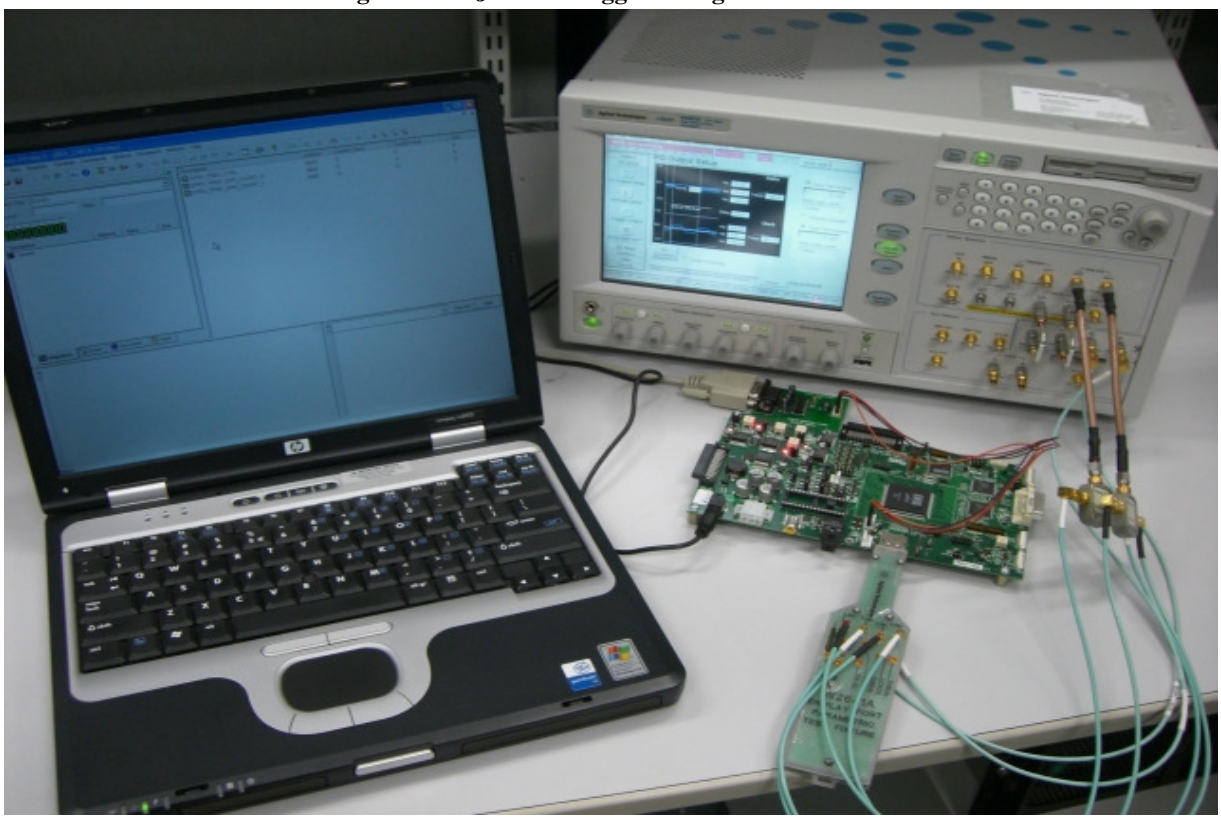

Figure A-3: Test Configuration with DUT and PC to read the PRBS7 error count

A.3- Basic SSG Calibration Setup

Figure A-4 shows the compliance point for sink tests as defined by reference [1]. The compliance point is TP3. This requires including the DisplayPort test fixture and the DisplayPort receptacle connector of the DUT into the calibration. As this is not feasible reference [1] requires calibration into a receptacle fixture as shown in figure A-4.

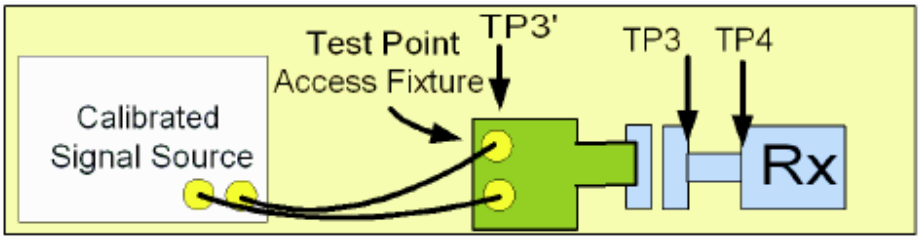

Figure A-4: Compliance points for sink test

In order to calibrate the test setup plug the test fixture (TF) into the receptacle test fixture (RTF). Terminate the aggressor signals with the 50 Ohm termination resistors and connect the data signal to the JMD.

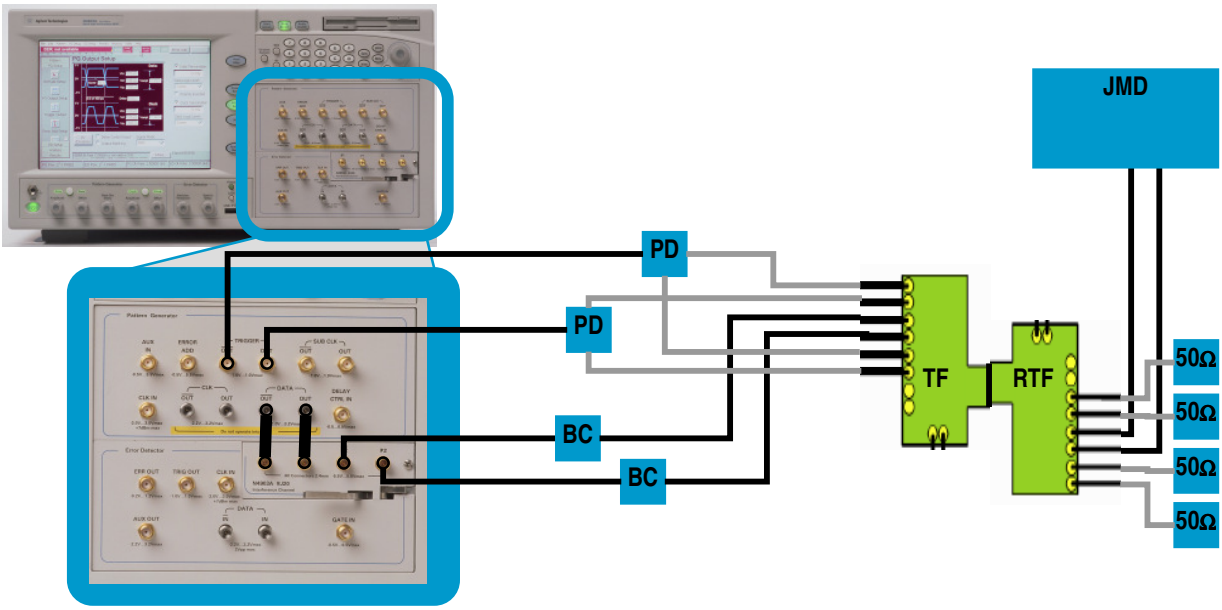

Figure A-4: Calibration setup

Figure A-5 shows a typical setup for calibration. In this example the cabling for the aggressor signals is not included.

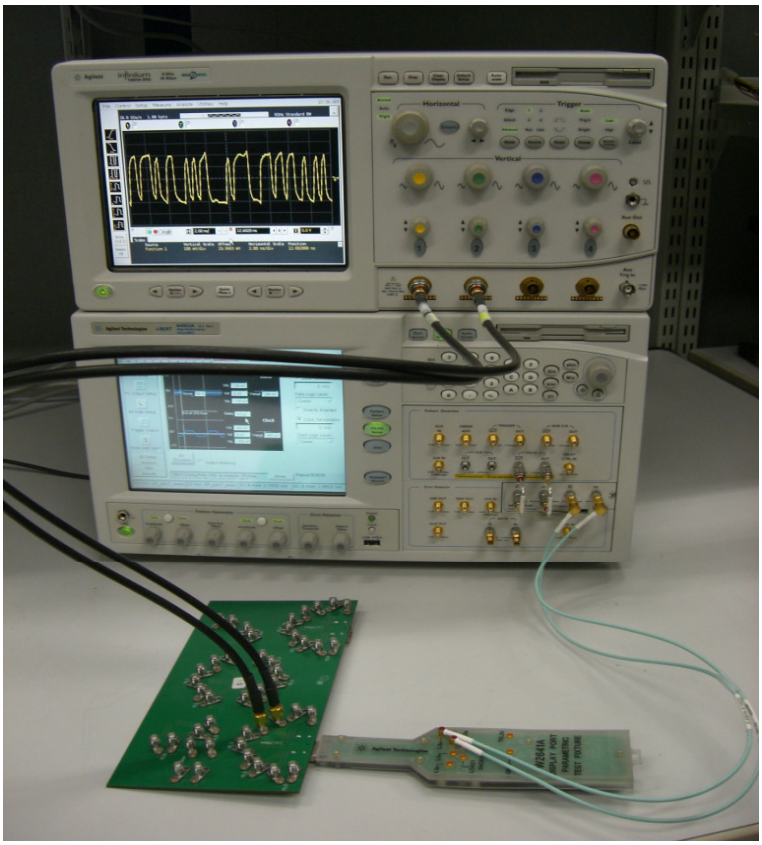

Figure A-5: Calibration setup with receptacle fixture (aggressors not shown)

A.4- Operating J-BERT During Test Execution

Load the J-BERT pattern sequencer as depicted in figure A-6. All required DisplayPort pattern are provided in the pattern storage in the DisplayPort folder.

The lower left corner of J-BERT's GUI always indicates which pattern is currently sent to the DUT.

The Error Add button in the upper right corner will be used during the test sequence to add a single bit error.

The Break button in the upper right corner will be used during the test sequence to switch between patterns.

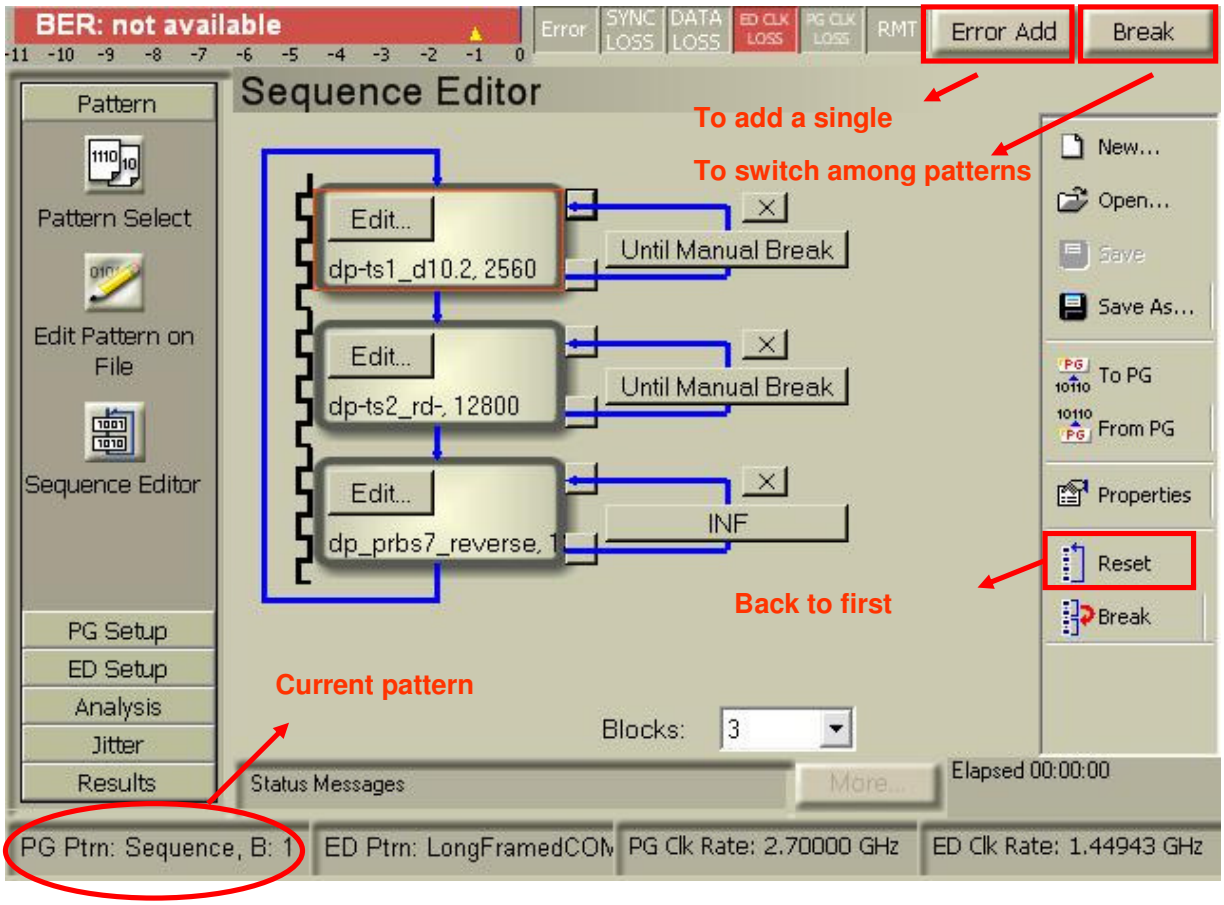

Figure A-6: J-BERT sequence editor

Appendix B – J-BERT Setup Calibration

Purpose: To calibrate the SSG parameters in accordance with [1] for performing the tests defined in this document.

References: None.

Last Modification: September 28, 2007

Discussion:

- Note that reference [1] is still a draft document. Some stress test parameters are not detailed there. For this case this MOI document will recommend appropriate settings.
- As explained in appendix A the aggressor signals will be turned on during setup calibration. Cross talk effects will be accounted to the Tj budget and Sj will be injected at lower levels not to exceed the Tj requirements given in reference [1].

B.1 - Introduction

The test setup has to be calibrated for all 7 tests individually (3 tests at RBR and 4 tests at HBR). As J-BERT is calibrated by itself the calibration data can be used as long as the setup i.e. cables and test fixture aren't changed.

B.2 – Calibrating the Pattern Generator Output Voltage

The output voltage has to be calibrated for each data rate. Set the data rate to 1.62GB/s for RBR and 2.7GB/s for HBR.

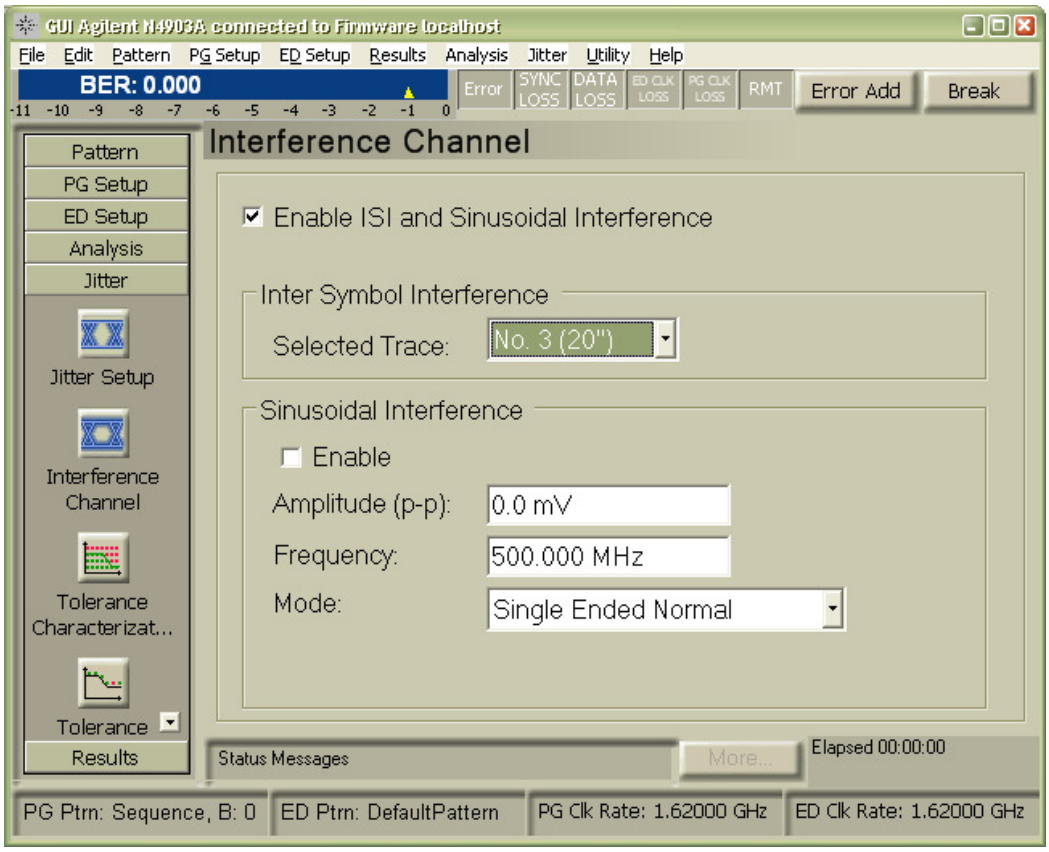

Figure B-1: Interference channel setup

Use ISI trace number 3 to inject the required amount of ISI as shown in figure B-1.

Make the Rj setting for the current data rate as shown in figure B-2:

- RBR: Rj(RMS)=17.8mUI
- HBR: Rj(RMS)=13.2mUI

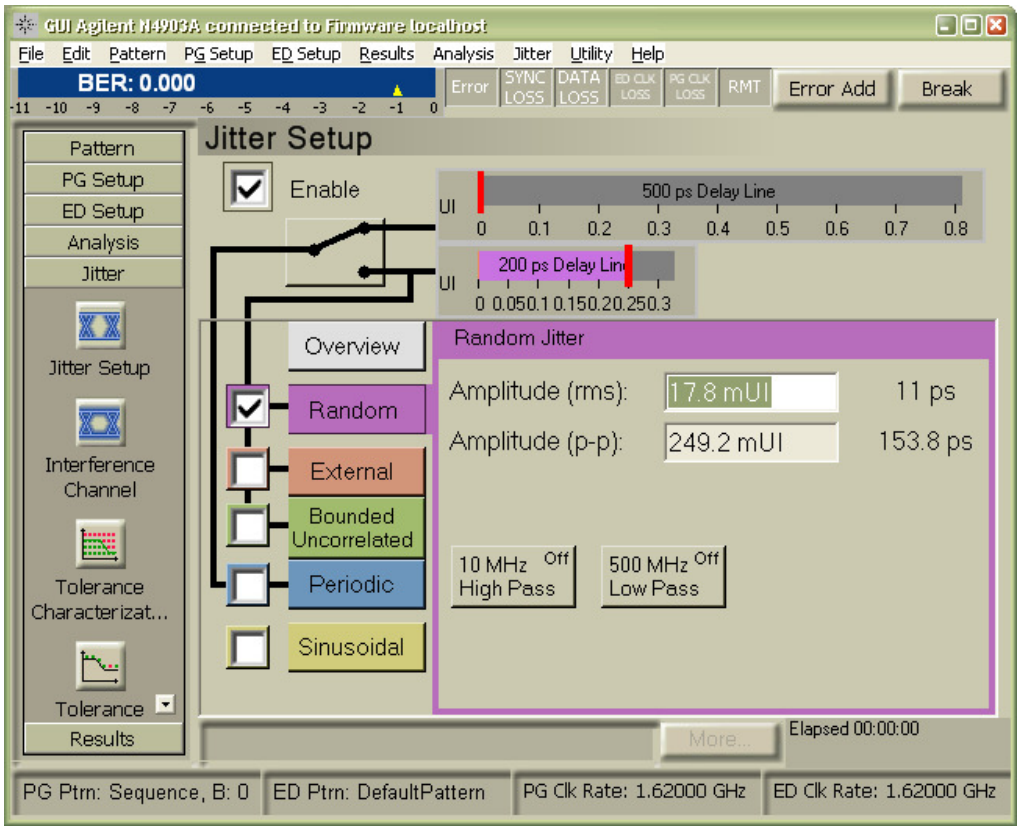

Figure B-2: Rj setup for RBR

Load the PRBS7 pattern from the DisplayPort pattern folder to the J-BERT pattern generator. Calibrate J-BERT's output voltage to the following values:

- RBR: 136mV(p-p)
- HBR: 150mV(p-p)

Therefore perform two mean histogram measurements on the lone bit in the PRBS7 pattern as shown in figure B-3 and figure B-4.

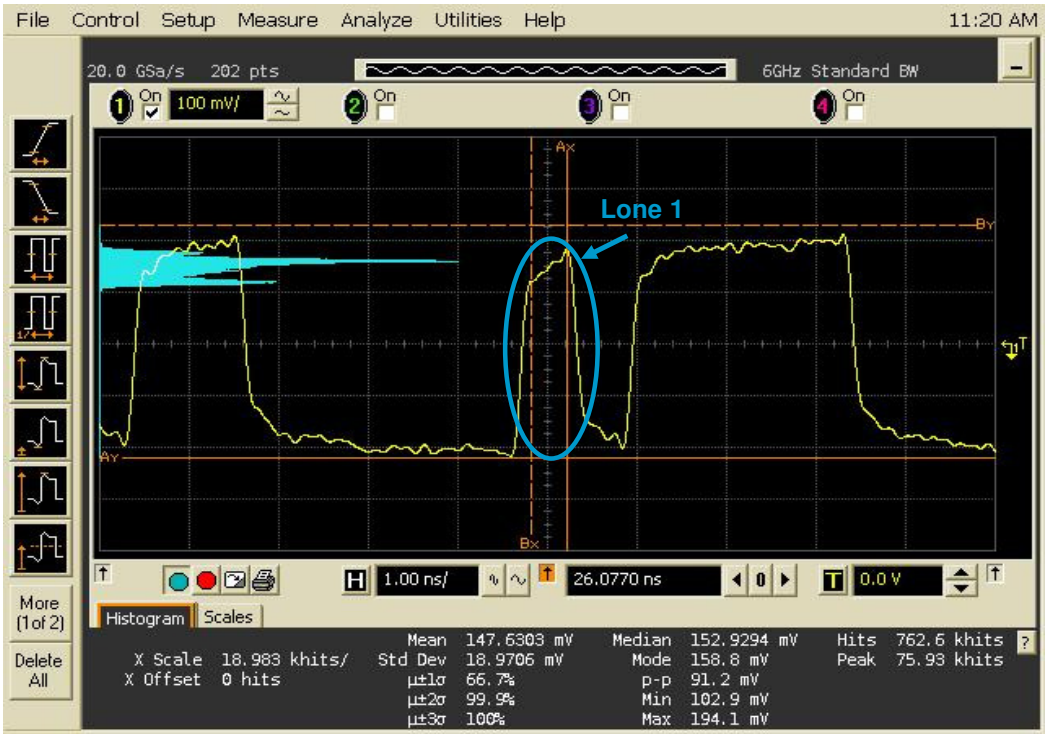

Figure B-3: Mean histogram measurement on a lone 1 bit

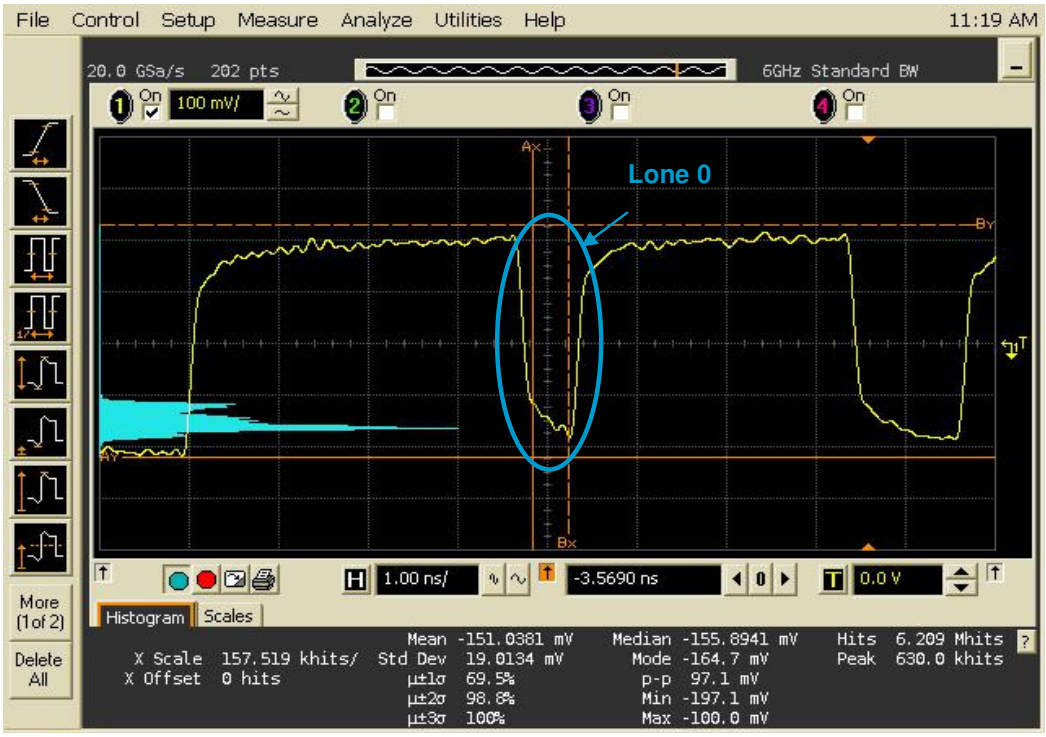

Figure B-4: Mean histogram measurement on a lone 0 bit

B.3 – Calibrating Jitter Settings

For each data rate use the above ISI and Rj settings and the calibrated output voltage. Start increasing Sj at the required frequency until the desired Tj is measured. Therefore perform a jitter measurement with the JMD as shown in figure B-5. Reference [1] details the desired Tj values in table 4-2 and table 4-3. Make sure that the data rate is adjusted for the 10MHz point according to table 4-1 in reference [1]. The following table summarizes the required calibration points:

Data Rate	Sj Frequency	Rj(RMS)	ISI	Required Tj
RBR = 1.62 GB/s	2 MHz	17.8 mUI	97 mUI	1268.9 mUI[1]
RBR + 350ppm = 1.620567 GB/s	10 MHz	17.8 mUI	97 mUI	589.9 mUI
RBR = 1.62 GB/s	20 MHz	17.8 mUI	97 mUI	546.9 mUI
HBR = 2.7 GB/s	2 MHz	13.2 mUI	161 mUI	1220.4 mUI
HBR + 350ppm = 2.700945 GB/s	10 MHz	13.2 mUI	161 mUI	541.4 mUI
HBR = 2.7 GB/s	20 MHz	13.2 mUI	161 mUI	498.4 mUI
HBR = 2.7 GB/s	100 MHz	13.2 mUI	161 mUI	484.4 mUI

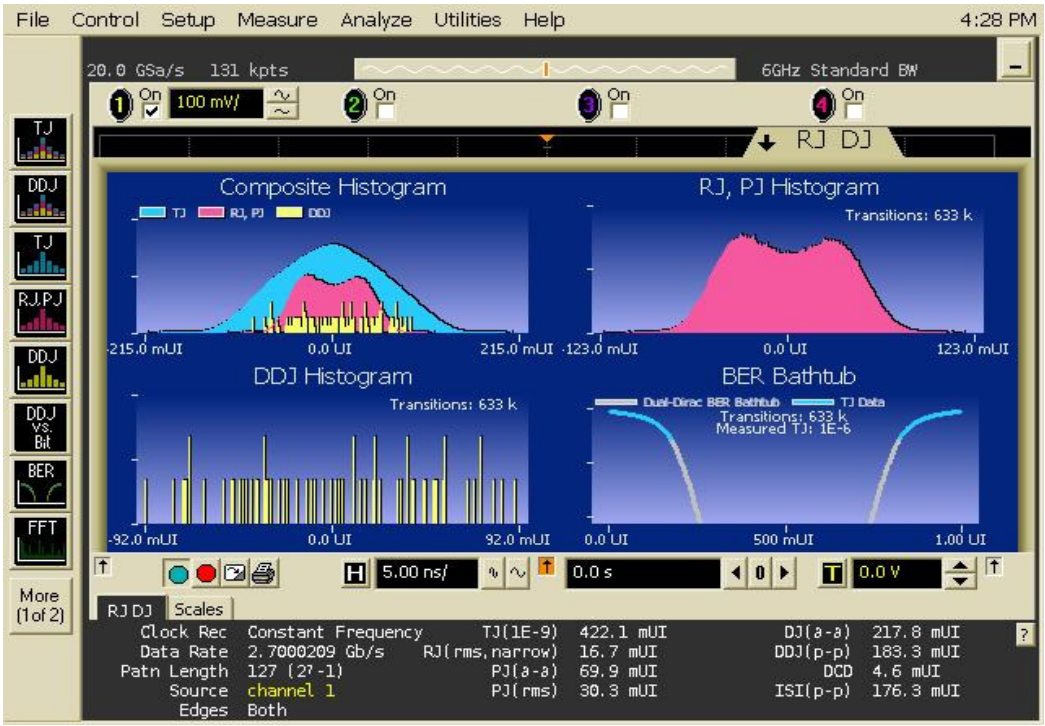

Figure B-5: Jitter measurement

[1] With the current firmware J-BERT may stay slightly below the required amount of Tj because the required amount of Sj is close to the current Sj generation capabilities at 2MHz/1.62GB/s. A firmware release is planned to provide additional jitter capabilities. Until this firmware is available J-BERT's clock may be modulated to inject larger amounts of Sj.

Appendix C – General Resource Requirements using the Agilent 81250 ParBERT

Purpose: To define the hardware/software requirements for performing the tests defined in this document using the ParBERT.

References: None.

Last Modification: November 3, 2007

Discussion:

- Reference [1] does not specify whether the aggressor signals shall be turned on during setup calibration. However test results have shown that cross talk effects add significant Tj to the stressed signal. Therefore the calibration setup will include the aggressor signals.

C.1 - Introduction

In order to perform receiver jitter tolerance testing on DisplayPort sink devices, several pieces of equipment are needed. The primary functional components are as follows:

Component	Function	Device/Model
Stressed Signal Generator (SSG)	Generates jittered/stressed test signal	Agilent 81250 ParBERT with the following modules: • 2x E4809A Central Clock • 3x N4874A 7G Generator • 1x 81250A-013 Firewire to VXI. • 1x 81250A-148 VXI Frame • 1xE4875A-ATO ParBERT User Software To generate the req. jitter the following instruments are req. • 1x NoiseCom Noise Source • 1xE4438C ESG (options:503,601,UNJ) or N5182A MXG (options: 654)
Required SSG accessories	Note: some accessories may be shipped with SSG	• 7x Agilent 11901C 2.4mm to 3.5mm Adapters • 1x Power Divider (e.g. Agilent 11636B) • 1x Agilent 1250-1744 Adapter N to SMA
Jitter Measurement Device (JMD)	Used to verify/calibrate SSG output	• Agilent Infiniium DSO81304A 13GHz Real-Time DSO • 1x Agilent 1169A 12 GHz Probe Amplifier • 1x Agilent N5380A SMA Probe Head • 1x Agilent N5400A EZJIT Plus
Adapter SMA(f) to SMA(f)	Used to connect the SMA cables with the SMA to SMP test cables.	6x Agilent 1250-1158

SMA test cables	Used to connect the SSG to PDs and the JMD for calibration	Agilent 15442-61601, or equivalent (set of 12 cables)
SMA to SMP test cables	Used to connect SSG with test fixture. Note: some SMA to SMP cables may be shipped with the DisplayPort test fixture.	Agilent E4809-61603 (6 required)
DisplayPort Test Fixture (TF)	Used to connect SSG with device under test	Agilent W2641A
DisplayPort Receptacle Test Fixture (RTF)	Used to calibrate test setup at compliance point	Molex part number tbd
Blocking Capacitor (BC)	Used to AC couple the SSC and DUT	Agilent 11742A (6 required)
50 Ohm termination resistors	Used during setup calibration & tests	Agilent N4912A (5 required)
BNC		
Test Automation Software	Used to automate all the tests and calibrations	Agilent N5990A with options 10, 155

C.2- Basic Test Setup

Figure C-1 shows the test setup with the ParBERT. Connect the output ports of the ESG and the Noise Source to the Power Divider. Connect the 3rd connector of the Power Divider with the Delay Control Input of the 1st (count from left to right) Generator Module. Use a SMA cable and a 2.4mm to 3.5mm Adapter to connect the Clk Output of the 1st Generator with the Clk Input port of the 2nd Central Clock Module. Connect the 6 DC-Blocks with the Generator using the 2.4mm to 3.5mm adapters. Connect 6 SMA cables to the DC-Blocks. Use the SMA(f) to SMA(f) Adapters to connect the SMA cables from the 2nd and 3rd Generator with the SMA to SMP cables, these are the adjacent lanes. Connect the SMA cables from the 1st Generator with the ISI Board and the other end of the ISI Board with 2 additional SMA cables. These 2 cables are also connected to the SMA to SMP cables. Connect these two SMA to SMP cables and connect it to the lane under test. Note that the TF is labeled for source test only. All lane numbers and signal polarity must be flipped. Connect the four remaining SMA to SMP cables connect to the lanes on the test fixture that are adjacent to the lane under test.

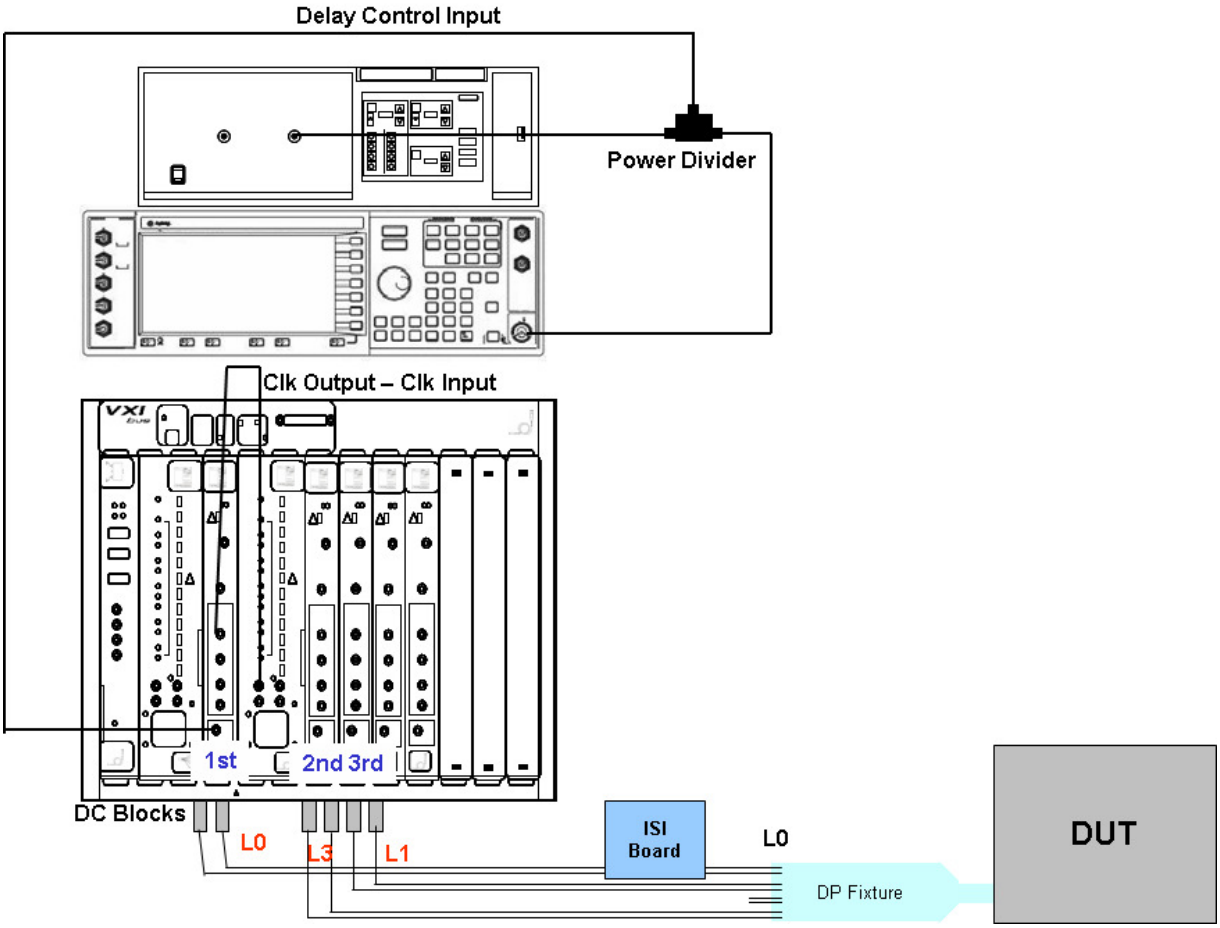

Figure C-1: Basic Test Configuration

Since there exists no standard Aux Control tool a vendor specific tool has to be used to operate the DUT. This tool may also utilize proprietary debug interfaces.

Note: All required changes in the connection will be displayed form the Agilent N5990A Test Automation Software prior the tests.

C.3- Basic SSG Calibration Setup

Figure C-2 shows the compliance point for sink tests as defined by reference [1]. The compliance point is TP3. This requires including the DisplayPort test fixture and the DisplayPort receptacle connector of the DUT into the calibration. As this is not feasible reference [1] requires calibration into a receptacle fixture as shown in figure C-3.

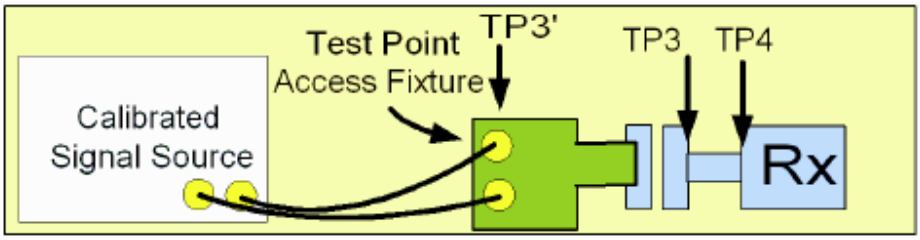

Figure C-2: Compliance points for sink test

In order to calibrate the test setup plug the test fixture (TF) into the receptacle test fixture (RTF). Terminate the aggressor signals with the 50 Ohm termination resistors and connect the data signal to the JMD.

Note: Adjacent signals are not shown in this image,however test have shown that this influences the test results and should be included during calibration.

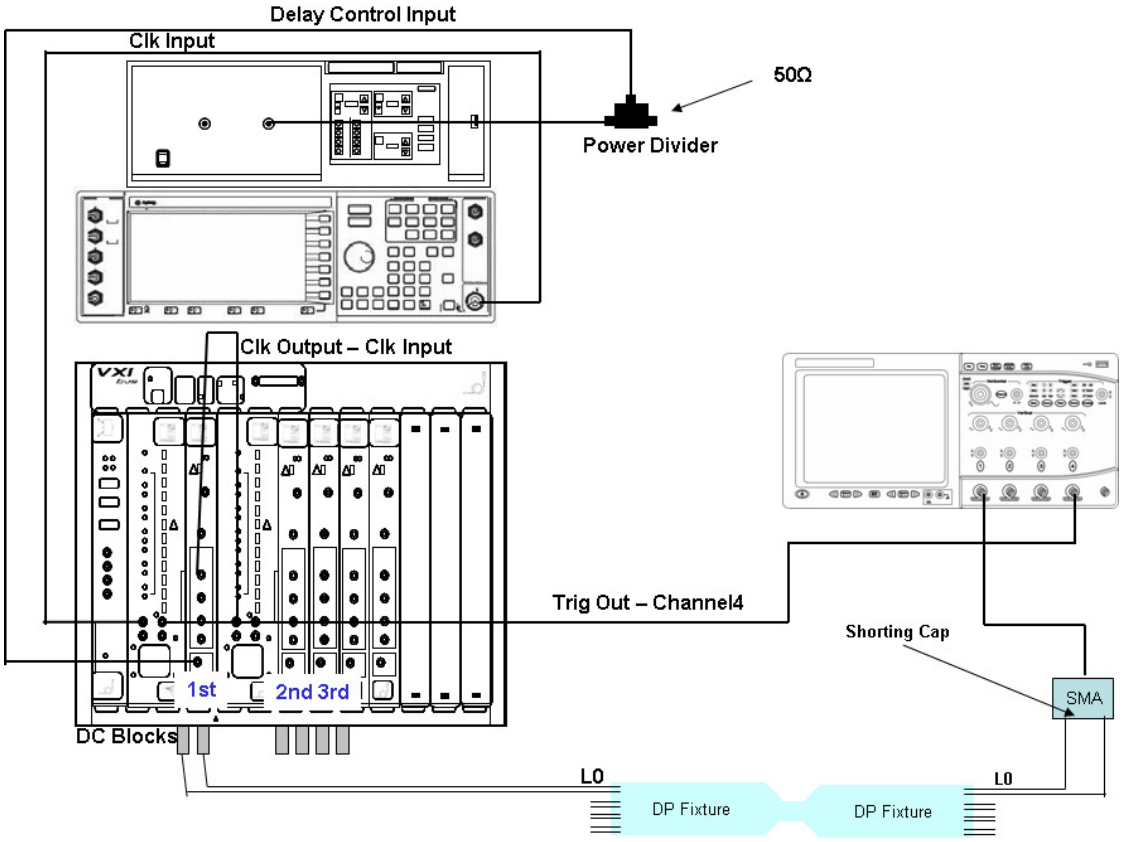

Figure C-3: Calibration setup

Appendix D – Using the Agilent N5990A Test Automation Software Option 155 together with the Agilent 81250 ParBERT

Purpose: Explain how to use the N5990A Test Automation Software Option 155 for the DisplayPort Sink Compliance tests.(N5990A is also referred to as 'ValiFrame')

References: None.

Last Modification: November 3, 2007

Discussion: The Agilent Test Automation Software N5990A-155 automates all manual steps required to calibrate the system and run the Sink Compliance Tests described in the DisplayPort Compliance Test Specification.

D.1 - General Setup

The Setup consists of the following components:

- Agilent 81250 ParBERT system with 3x7G generators in two clock groups as SSG
- Agilent E4438C signal generator as clock and jitter source
- NoiseCom noise generator as Rj source
- Agilent DSO80000 series oscilloscope to calibrate the SSG (as JMD)
- PC running the N5990A software and the ParBERT firmware.

The following figure shows the cabling of the instruments.

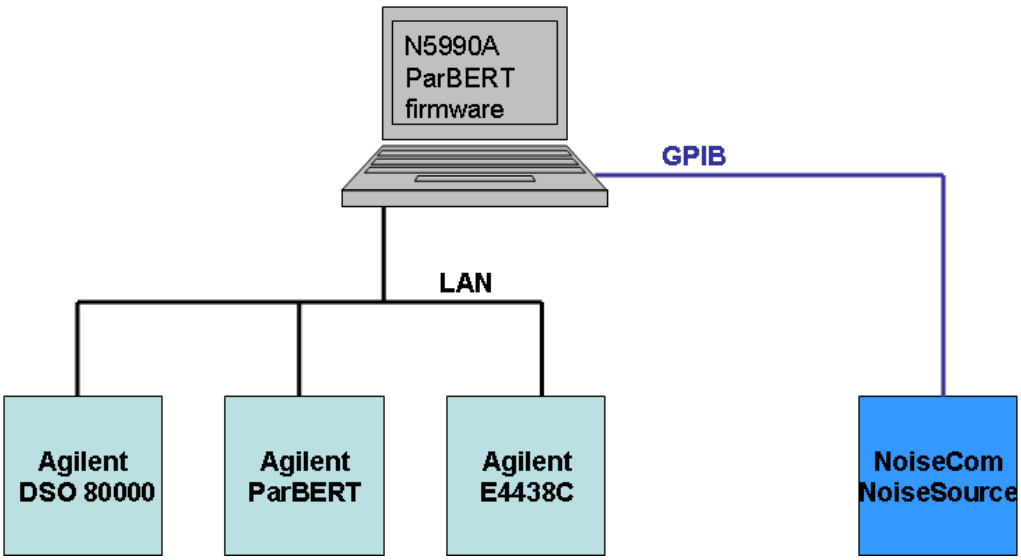

Figure D-1: General Setup

D.2 – Installing and Configuring the Software

Before installing the Agilent N5990A Test Automation Software Option 155 the following components should be installed on the Host PC:

- Microsoft .NET Framework 1.1
- Microsoft .NET Framework 2.0
- Microsoft Excel 2003 or higher
- Agilent IO Libraries Suite 14.2
- Agilent 81250 User Software
- Agilent T&M Toolkit Redistributable Package 1.1

After installing Valiframe "Valiframe Station Configuration" should be first, to setup all the instrument addresses.

- Start Valiframe Station Configuration
- Select "DisplayPort Station"

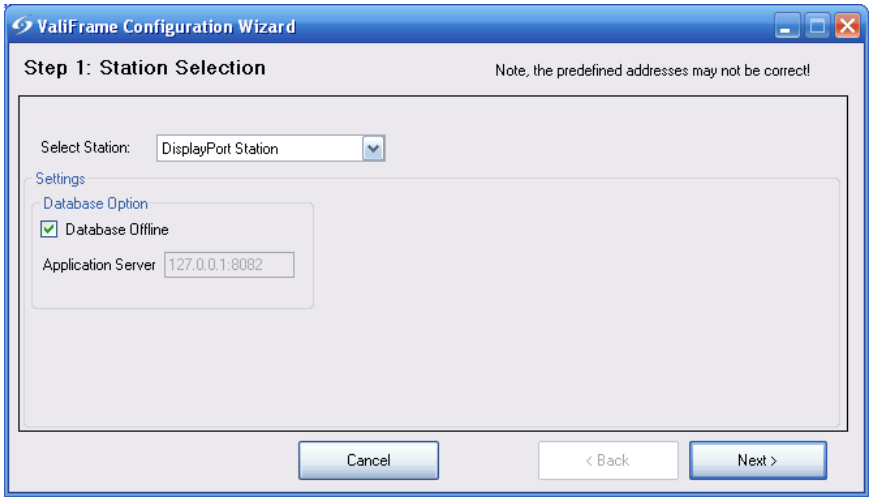

Figure D-2: Configuration Wizard

- Click "Next!"

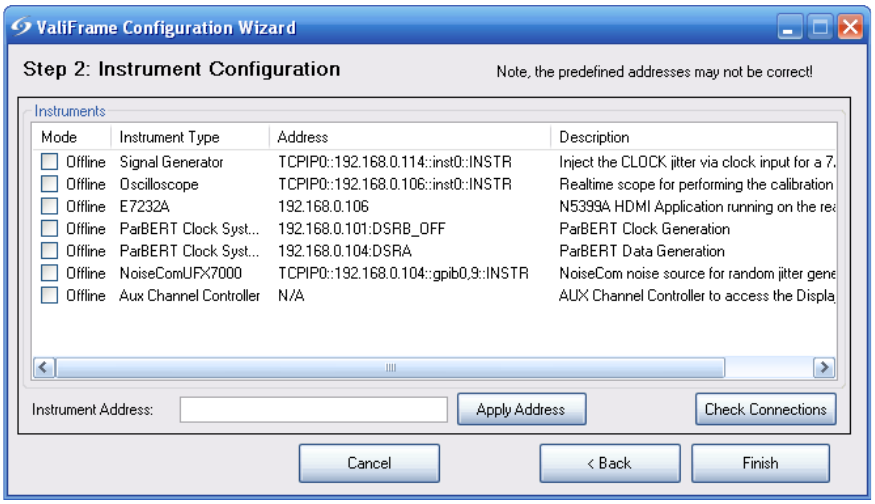

Figure D-3: Configuration Wizard

- Make sure, that all Offline Flags are unchecked and each instrument has its right address.
- You can test the connection to the instruments by clicking on the "Check Connections" button. All Online instruments will than be tested, if ValiFrame can connect to them.
- Once you have successfully setup the connections, you can leave the program by licking on the "Finish" button. All settings will be stored and as long as you don't change anything in the setup

D.3 – Calibrating the Setup

- Start ValiFrame

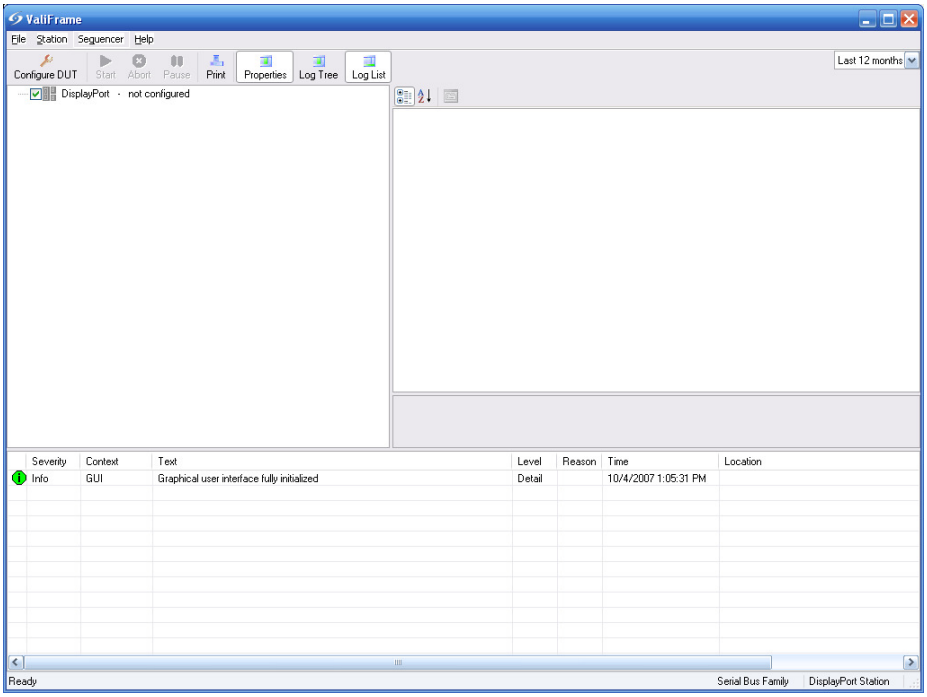

Figure D-4: ValiFrame Startup Screen

- Press "Configure DUT"

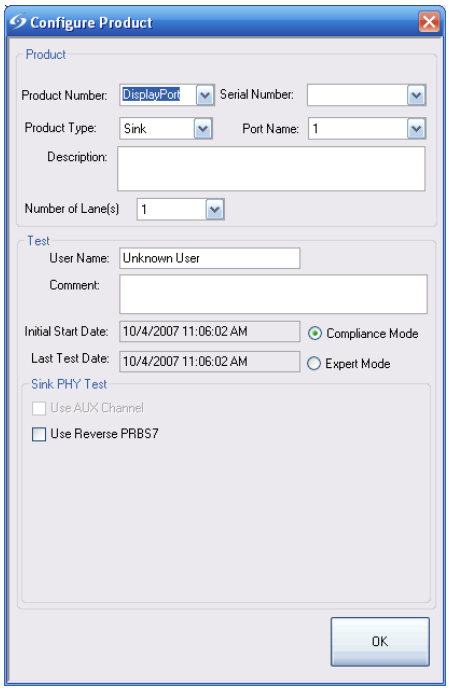

Figure D-5: Configure DUT Dialog

- Select the number of lanes and press OK.

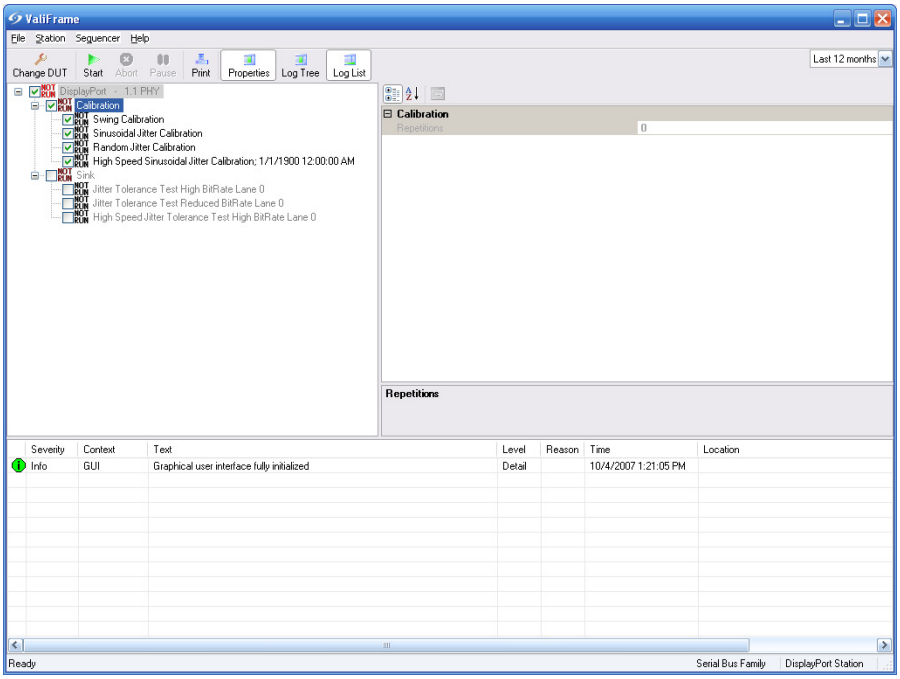

Figure D-6: Running Calibrations

- Select the Calibration node to automatically select all child nodes.
- Press the "Start" button to start the calibration process
- ValiFrame will calibrate the Rj, Sj and the swing voltage of the SSG. ValiFrame uses the same calibration process described in "Appendix B – J-BERT Setup Calibration"
- Prior the tests ValiFrame will show you a connection diagram, how to connect all the instruments. If two tests require the same connection and these tests are executed after each other, the connection diagram will only be visible once.
- After all calibration procedures were finished successful (show a green happy smiling indicator next to their checkbox) you have successful finished the calibration of the SSG.
- The calibration data will be stored and used for all the tests. If you exchange parts of the SSG setup, you should rerun the calibration procedures. In advance it is highly recommended to rerun the calibration procedures form time to time to eliminate the influence of slightly drifting instruments.

C.4 – Running the Compliance Tests

- Deselect the Calibration node and select the Sink node instead.

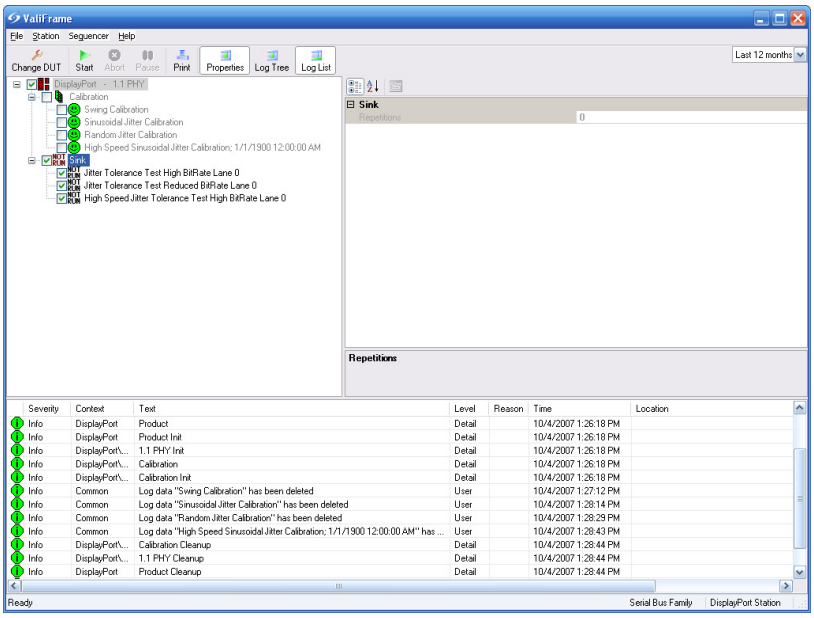

Figure D-7: Running Tests

- Depending on the number of lanes you have specified for your DUT, this list has a different amount of test procedures. For each lane there are 3 procedures listed. The Jitter Tolerance Test (JTT) with reduced bit rate, the JTT with high bit rate and Sj frequencies from 2 MHz to 20 MHz and the JTT with 100 MHz Sj.
- ValiFrame will show again connection diagrams every time a change in the connection is required.
- After the tests were finished the indicator next to the checkbox of each procedure shows the test results as an overview. You can double click on the test items to open the Excel sheet containing the detailed test results

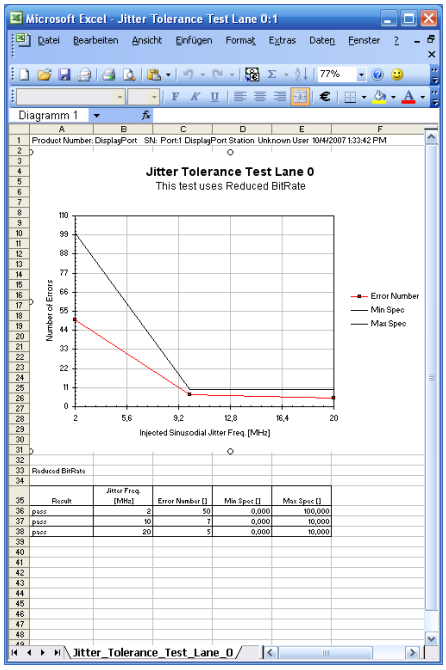

Figure D-8: Test Result

- After you have completed all tests, you can save an Excel workbook containing all the test result sheets by clicking the File > Save as workbook menu option.